Listing of the Claims

1. (Currently Amended) A liquid crystal display, comprising:

a signal processor for generating and outputting a first image signal, a second image signal and a driving control signal using an image data, a main control signal, and a power source all of which are supplied from an image supplying source, the driving control signal including a source driving control signal and a gate driving control signal;

a data signal driver for generating and outputting a data signal from the first or second image signal and the source driving control signal all of which are input from said signal processor;

a printed circuit board having a plurality of wires for transmitting the signals and/or voltages of said signal processor to said data signal driver;

a gate signal driver for generating and outputting a gate signal from the gate driving control signal of said signal processor; and

a liquid crystal display panel for displaying an image formed by receiving the data signal from said data signal driver and the gate signal from said gate signal driver,

wherein the plurality of wires comprises a first group of wires for transmitting the first image signal and a second group of wires for transmitting the second image signal, and the first group of wires are entirely spaced apart from the second group of wires, and two groups of the data signal driver outputting simultaneously a data signal from the first

image signal and the second image signal, one of which is the left-side of the signal processor and the other of which is the right-side of the processor.

2. (Previously Presented) The liquid crystal display of claim 1, wherein the data signal driver comprises at least four source drive integrated circuits and is physically, electrically connected to said liquid crystal display panel by a connecting member mounting the source drive integrated circuits one to one, wherein the connecting member includes a first group of connecting member and a second group of connecting member symmetrically separated by the middle of the printed circuit board, the first group of connecting member being connected with the first group of wires and the second group of connecting member being connected with the second group of wires.

3. (Original) The liquid crystal display of claim 2, wherein the first image signal includes a first clock signal and the second image signal includes a second clock signal, and the first clock signal and the second clock signal have a frequency half of a clock signal frequency supplied from the image supplying source.

4. (Original) The liquid crystal display of claim 2, wherein the first image

signal includes a first shift signal and the second image signal includes a second shift signal, the first shift signal and the second shift signal being respectively applied to a source drive integrated circuit of a corresponding group of the source drive integrated circuits such that the group of the source drive integrated circuits have the same phase.

5. (Previously Presented) The liquid crystal display of claim 2, wherein the first image signal includes a first drive signal and the second image signal includes a second drive signal, the first drive signal and the second drive signal being respectively applied to a source drive integrated circuit of a corresponding group of the source drive integrated circuits such that the group of the source drive integrated circuits has the same phase.

6. (Original) The liquid crystal display of claim 2, wherein the first group of wires and the second group of wires are branched from an wire aggregation including a plurality of wires at a selected position.

7. (Original) The liquid crystal display of claim 1,wherein said printed circuit board is a source printed circuit board.

8. (Original) The liquid crystal display of claim 1,wherein the first group of wires and the second group of wires are arranged in a T-shape on said

printed circuit board.

9. (Previously Presented) A liquid crystal display, comprising:

a signal processor for generating and outputting a first image signal, a second image signal, and a driving control signal using an image data, a main control signal, and a power source all of which are supplied from an image supplying source, the driving control signal including a source driving control signal and a gate driving control signal;

a data signal driver for generating and outputting a data signal from the first or second image signal and the source driving control signal all of which are input from said signal processor;

a printed circuit board having a plurality of wires for transmitting the signals of said signal processor to said data signal driver;

a gate signal driver for generating and outputting a gate signal from the gate driving control signal of said signal processor; and

a liquid crystal display panel for displaying an image formed by receiving the data signal from said data signal driver and the gate signal from said gate signal driver, wherein the plurality of wires comprises a first group of wires for transmitting the first image signal and a second group of wires for transmitting the second image signal, and the first group of wires are entirely spaced apart from the second group of wires, and the first image signal and the second image signal being transmitted

simultaneously, and wherein the data signal driver comprises at least four source drive integrated circuits and is physically, electrically connected to said liquid crystal display panel by a connecting member mounting the source drive integrated circuits one to one, wherein the connecting member includes a first group of connecting member and a second group connecting member, the first group of connecting member being connected with the first group of wires and the second group of connecting member being connected with the second group of wires.

10. (Previously presented) The liquid crystal display of claim 9, wherein the first image signal includes a first clock signal and the second image signal includes a second clock signal, and the first clock signal and the second clock signal have a frequency half of a clock signal frequency supplied from the image supplying source.

11. (Previously presented) The liquid crystal display of claim 9, wherein the first image signal includes a first shift signal and the second image signal includes a second shift signal, the first shift signal and the second shift signal being respectively applied to a source drive integrated circuit of a corresponding group of the source drive integrated circuits such that the group of the source drive integrated circuits have the same phase.

12. (Previously presented) The liquid crystal display of claim 9, wherein the first group of wires and the second group of wires are branched from an wire aggregation including a plurality of wires at a selected position.

13. (Previously presented) The liquid crystal display of claim 1, wherein edges of the printed circuit board and the signal processor is overlapped with each other.

14. (Previously presented) The liquid crystal display of claim 13, wherein an anisotropic conductive film is interposed between the overlapped edges of the printed circuit board and the signal processor.

15. (Currently Amended) The liquid crystal display of claim 13, wherein the overlapped portion of the printed circuit board and the signal processor ~~has~~ is narrower ~~width~~ than ~~a~~ the remaining portion of the printed circuit board.

16. (Previously presented) The liquid crystal display of claim 13, wherein the overlapped portion of the printed circuit board and the signal processor has narrower width than a remaining portion of the signal processor.

17. (Previously presented) The liquid crystal display of claim 1, wherein

the printed circuit board comprises a plurality of parts.

18. (Previously presented) The liquid crystal display of claim 17, wherein the parts comprises a voltage supplying part, a gate voltage generating part, a gray scale voltage generating part and a timing controller.

19. (Previously presented) The liquid crystal display of claim 1, wherein the printed circuit board is formed on a different substrate from a thin film transistor substrate of the liquid crystal display panel.

20. (Previously presented) The liquid crystal display of claim 1, wherein the first and second image signals comprises a first clock signal and a second clock signal, respectively, and the first and second clock signals have the same phase and frequency with each other.

21. (Previously presented) The liquid crystal display of claim 1, wherein the wires are formed on one surface of the printed circuit board.

22. (Previously presented) The liquid crystal display of claim 9, wherein edges of the printed circuit board and the signal processor is overlapped with each other.

23. (Previously presented) The liquid crystal display of claim 22, wherein an anisotropic conductive film is interposed between the overlapped edges of the printed circuit board and the signal processor.

24. (Previously presented) The liquid crystal display of claim 22, wherein the overlapped portion of the printed circuit board and the signal processor has narrower width than a remaining portion of the printed circuit board.

25. (Previously presented) The liquid crystal display of claim 22, wherein the overlapped portion of the printed circuit board and the signal processor has narrower width than a remaining portion of the signal processor.

26. (Previously presented) The liquid crystal display of claim 9, wherein the printed circuit board comprises a plurality of parts.

27. (Previously presented) The liquid crystal display of claim 26, wherein the parts comprises a voltage supplying part, a gate voltage generating part, a gray scale voltage generating part and a timing controller.

28. (Previously presented) The liquid crystal display of claim 9, wherein the first and second image signals comprises a first clock signal and a second clock signal, respectively, and the first and second clock signals

have the same phase and frequency with each other.

29. (Previously presented) The liquid crystal display of claim 9, wherein the wires are formed on one surface of the printed circuit board.